

# From Nano-Scale to Peta-Scale

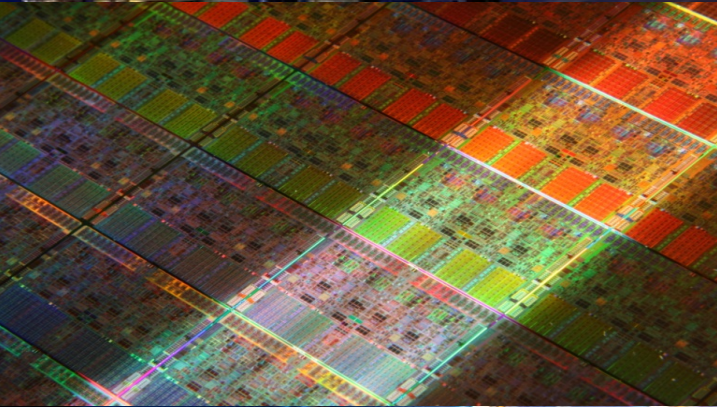
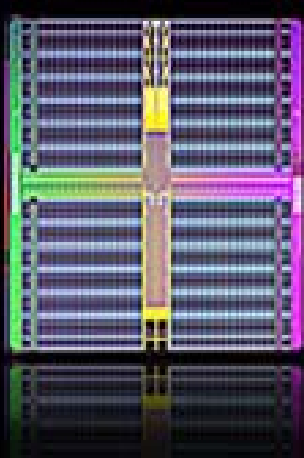
12 June 2009  
Herbert Cornelius  
Intel EMEA

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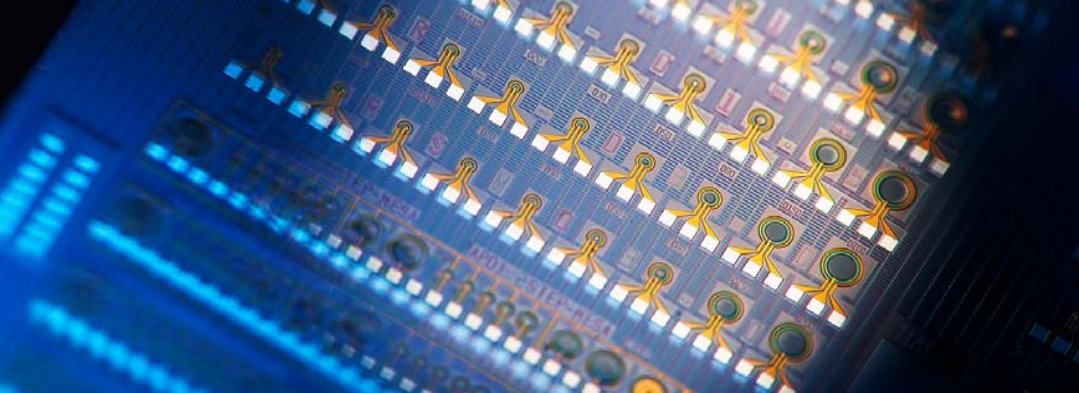
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Investing  
\$7B into  
32nm fabs



## STARING INTO THE ABYSS? DON'T BLINK.

How do we respond to the deepest economic crisis of a generation? Imagine a company with the nerve to look this challenge in the eye and invest \$7 billion of its own money in America right now. Crazy? We think it's foresight.

Intel was in Washington this week to announce the single largest capital investment in a new manufacturing cycle in its history. The company is putting big money into factories that will produce next-generation 32 nanometer chips, tiny engineering marvels that will generate economic returns far beyond one company or industry. These factories are the lifeblood of communities in Oregon, New Mexico and Arizona, a major part of Intel sustaining 45,000 highly skilled jobs in America. We believe economic stimulus starts with words like *build* and *invest*.

The commitment to new manufacturing capacity is, we think, a fundamental expression of faith in technology and faith in the future of the United States. It is not a blind faith, but a faith buttressed by years of experience.

*Faith in technology.* Just as American leaders like Teddy Roosevelt looked way into the future, our company has the confidence to invest in the downturns, knowing that

is the surest path to a healthier tomorrow. These state-of-the-art factories will produce a whole new generation of extremely capable, yet ultra low power chips. These chips will animate a new class of computer servers, thin and light notebooks and a range of devices that deliver a rich Internet experience in your pocket or purse. We have a bedrock conviction that we will lift ourselves out of the economic funk not with today's products, but with tomorrow's.

*Faith in the U.S.* Intel is a global enterprise, with important factories and operations all over the world. While 75 percent of our chips are destined for export to world markets, we actually *make* 75 percent of the chips in U.S. factories. It makes good sense to upgrade manufacturing capacity where we have the skills, capital equipment and existing investments to accelerate our time to market and maintain process leadership.

Come join us as we convene an important conversation over the next year. Partnering with The Aspen Institute and other thought leaders, Intel will stimulate a discussion about the importance of investing in technology to get the economy growing again.

[intel.com/InnovationEconomy](http://intel.com/InnovationEconomy)

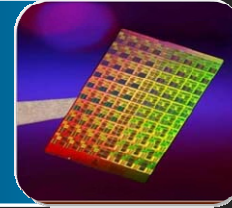


# Intel in High-Performance Computing



Dedicated,  
renowned  
applications  
expertise

Teraflops  
Research  
Chip



Broad Software  
tools  
portfolio

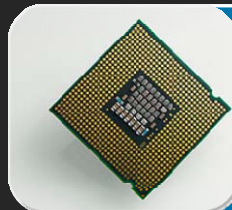
Defined  
HPC  
application  
platform



Large scale  
clusters  
for test &  
optimization



Manufacturing  
Process  
Technologies



Leading  
performance,  
performance/watt

Platform  
building  
blocks

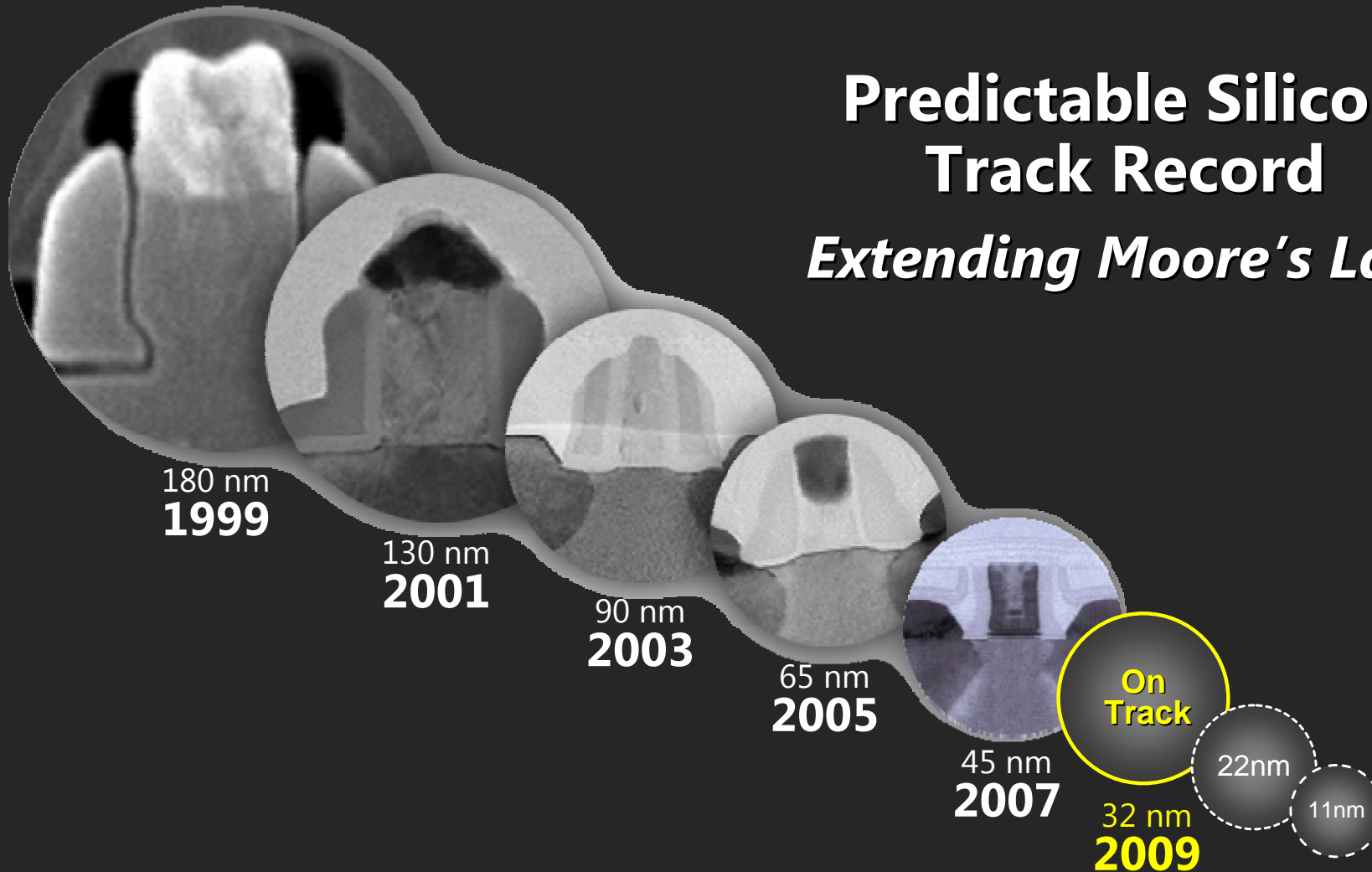


**A long term commitment to the HPC market segment**



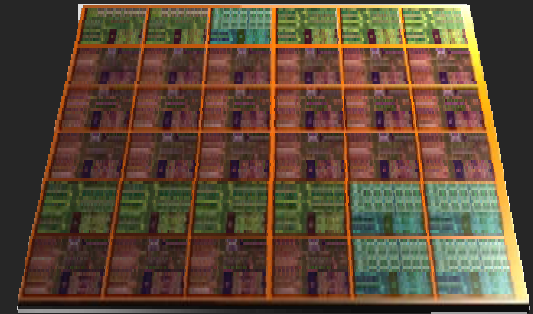
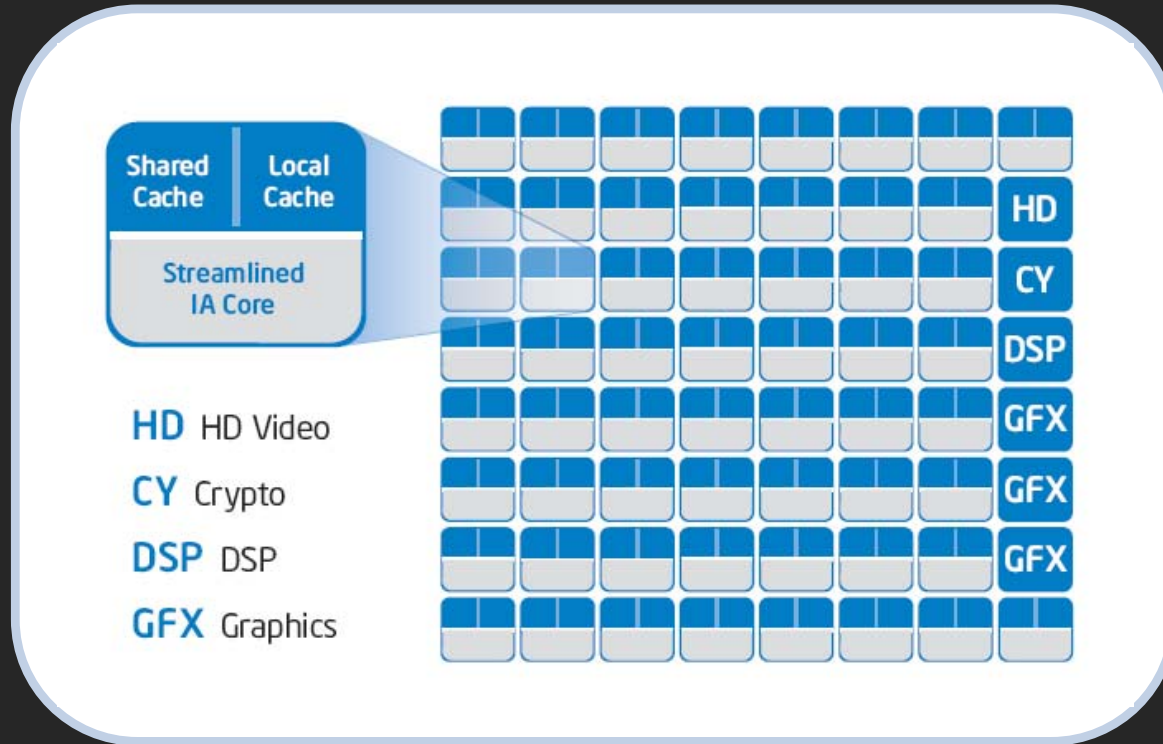
# Predictable Silicon Track Record

## *Extending Moore's Law*





# Multi/Many-Core Chip Research

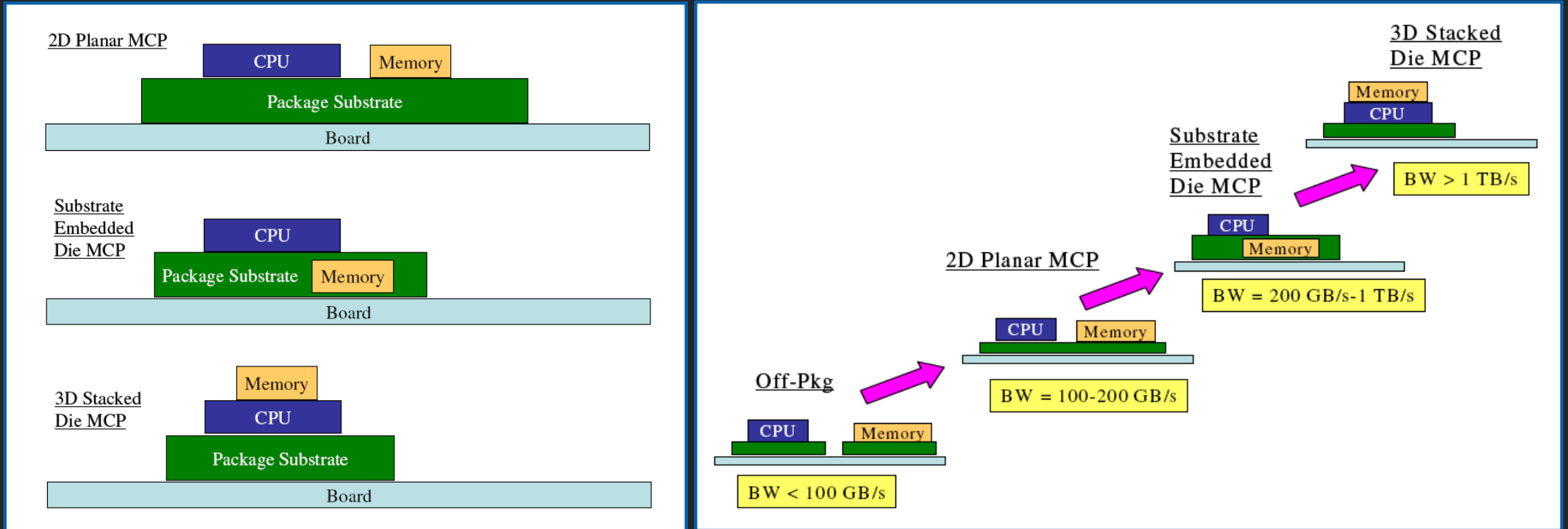


Future tera-scale chips could use an array of tens to hundreds of cores with reconfigurable caches, as well as special-purpose hardware accelerators utilizing a scalable on-die interconnect fabric.

Potential future options, no indication of actual product or development, subject to change without notice.



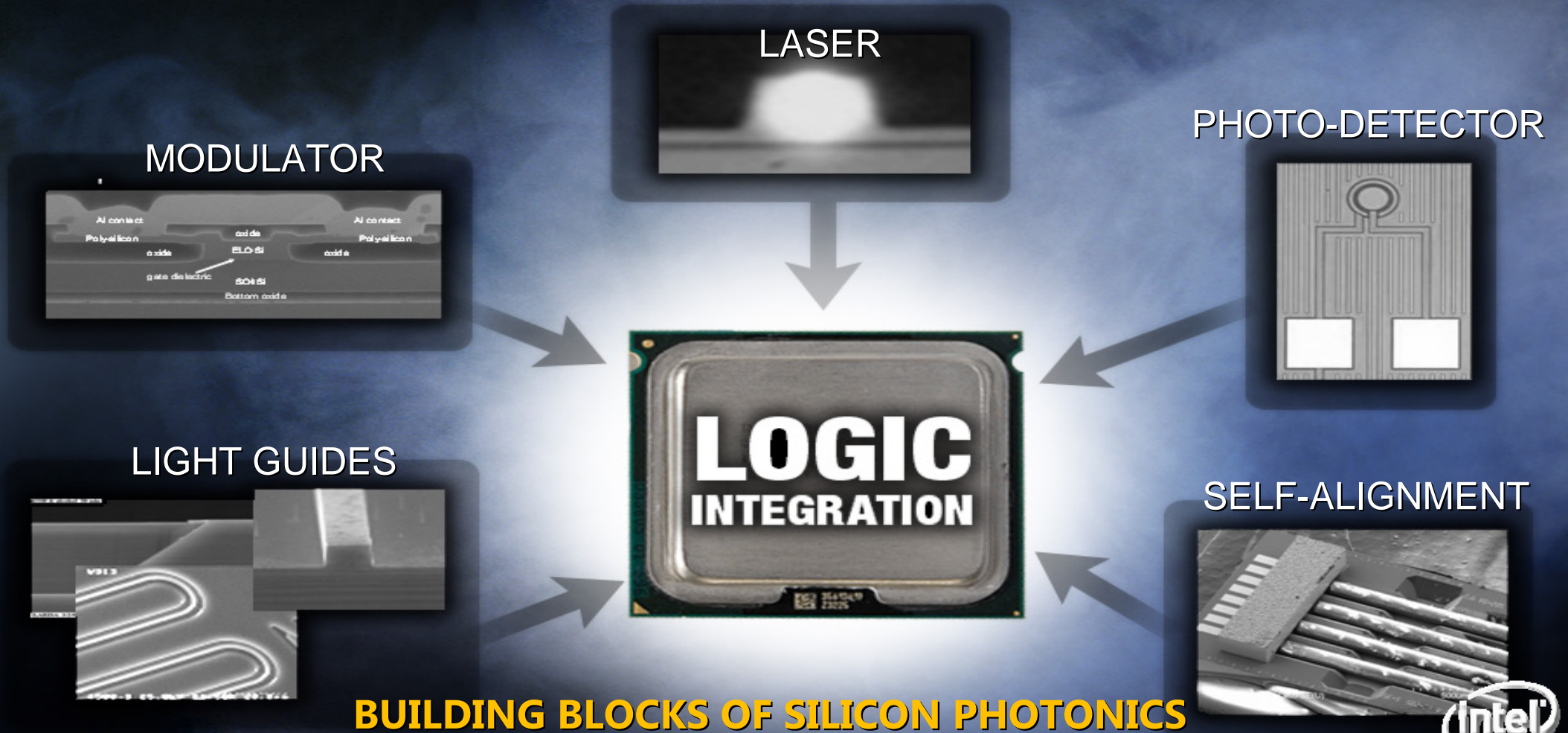
# Memory and CPU package architectures for addressing bandwidth challenges



Package Technology to Address the Memory Bandwidth Challenge for Tera-scale Computing, Intel Technology Journal, Volume 11, Issue 3, 2007



# TERABITS OF I/O-THROUGHPUT



**BUILDING BLOCKS OF SILICON PHOTONICS**





# Intel Technology is Changing HPC

Performance, Energy Efficiency, Reliability, TCO

**Extreme  
Performance**

**Increased  
Reliability**

**Power  
Efficient**

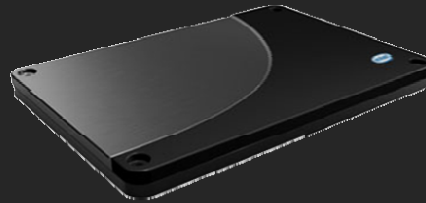
**Reduce  
System Cost**

Processor



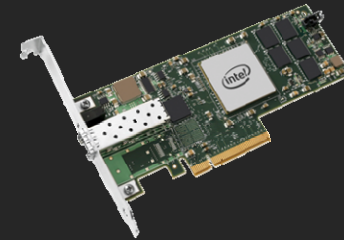
**Scalable Performance  
and Energy Efficiency**

Solid State Disk



**Optimize Performance for  
I/O Intensive Apps and  
Boot Drive Replacement**

10GbE

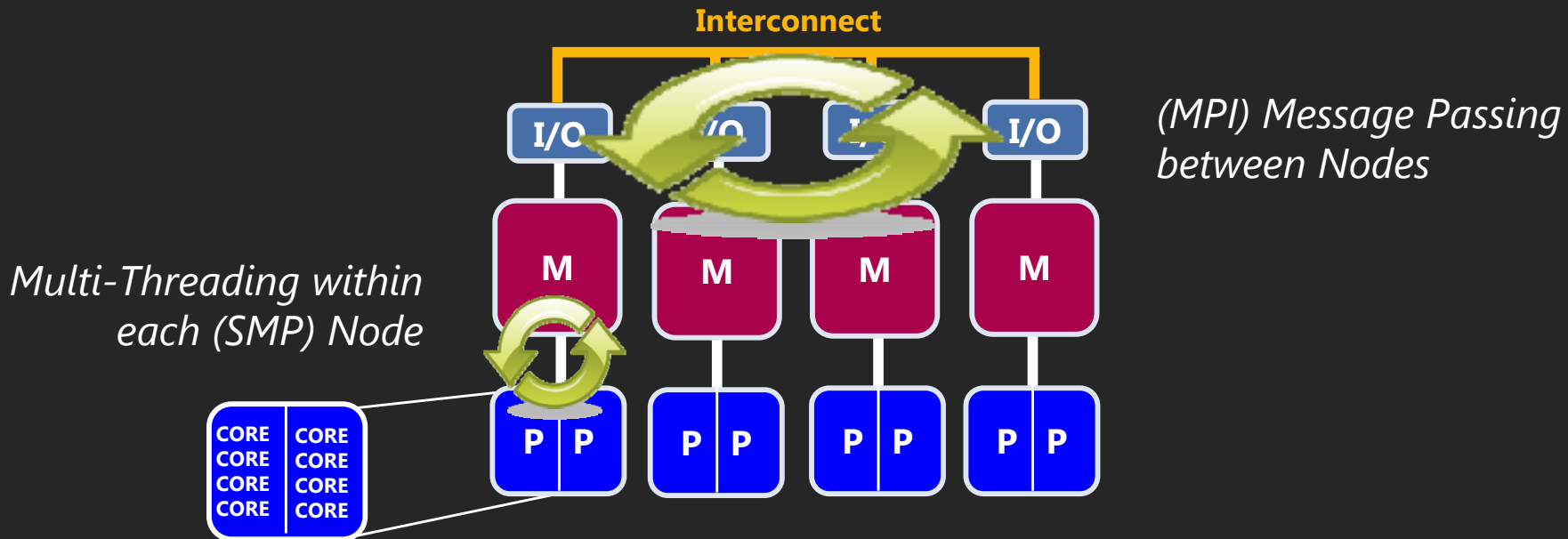


**Bridging the Gap  
Between  
1GbE and Infiniband®**



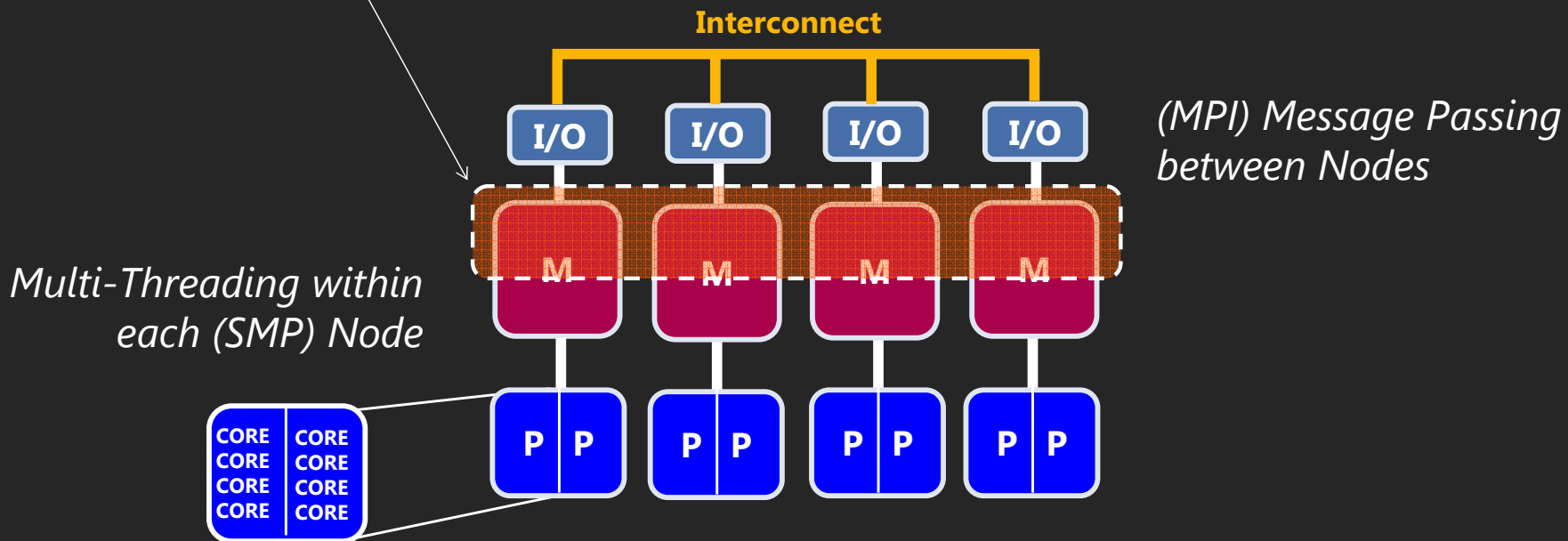
# HPC Architecture

## CLUSTER OF SHARED MEMORY NODES



# HPC Architecture

## Partitioned Global Arrays (PGAS)





# Some (HPC) Technology Trend Predictions

Processor #Cores

2 ▶ 4 ▶ **8** ▶ O(10) ▶ O(100)

SIMD

64b ▶ **128b** ▶ 256b ▶ 512b

Memory

DDR2 ▶ **DDR3** ▶ DDR4

I/O

PCI ▶ PCIe ▶ **PCIe Gen2** ▶ PCIe Gen3

Storage

HDD ▶ **SSD**

Infiniband\*

SDR ▶ DDR ▶ **QDR** ▶ EDR

GbE

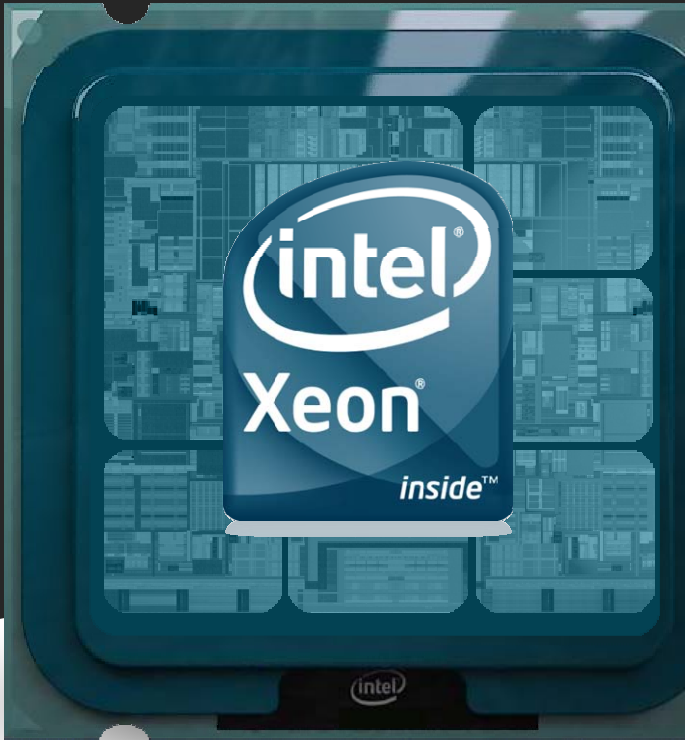
0.1 ▶ 1 ▶ **10** ▶ 40 ▶ 100

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# Levels of Parallelism

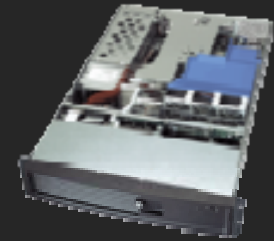


Clustering

Multi-Threading

SIMD

ILP





# Market Leading Software Development Tools

*Message Passing  
Multi-Threading  
Vectorization  
Optimization*


**Compilers**



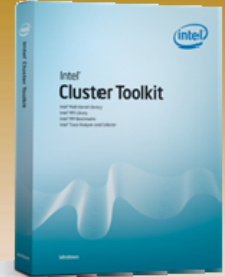
**Libraries**



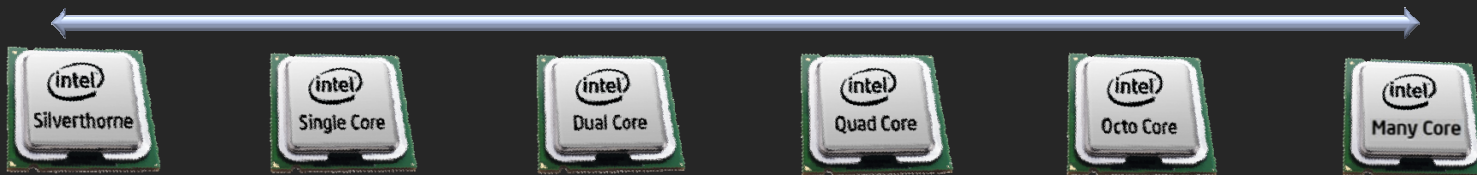
**Analyzers**



**Clusters**



*Performance  
Confidence  
Analysis  
Implementation*



Performance | Compatibility | Support | Productivity | Cross-Platform

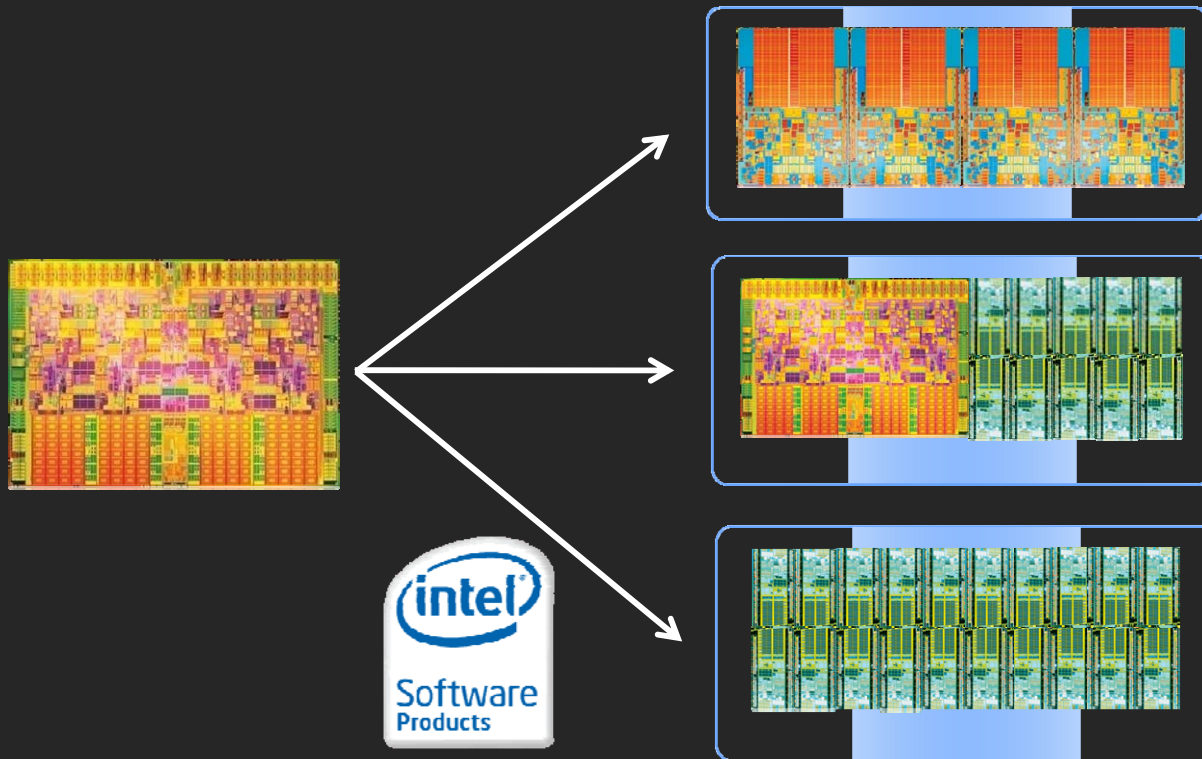
[www.intel.com/software](http://www.intel.com/software)







# Forward Scaling Software Tools Vision



**Employ uniform  
development tools  
across all architectures**

**Single Source Code  
Flexible  
Programmability**

*Data-Parallelism (SIMD)*

*Thread-Parallelism (MT)*

*Message Passing (MPI)*

Potential future options, no indication of  
actual product or development, subject to change without notice.



# Programming Languages - Ct <sup>throughput</sup>

*All Programs Become Parallel Programs*

**Beta in 2H09**

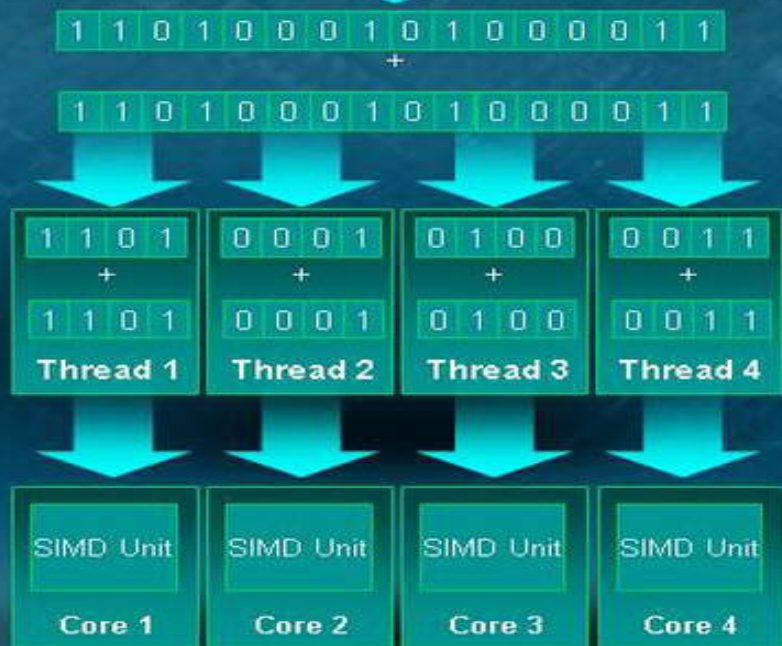
```
TVEC<F32> a(src1), b(src2);  
TVEC<F32> c = a + b;  
c.copyOut(dest);
```

User Writes Serial-Like  
Core Independent C++ Code

Primary Data Abstraction is the Nested Vector  
Supports Dense, Sparse, and Irregular Data

Ct Parallel Runtime:  
Auto-Scale to Increasing Cores

Ct JIT Compiler:  
Auto-vectorization, SSE, AVX, Larrabee



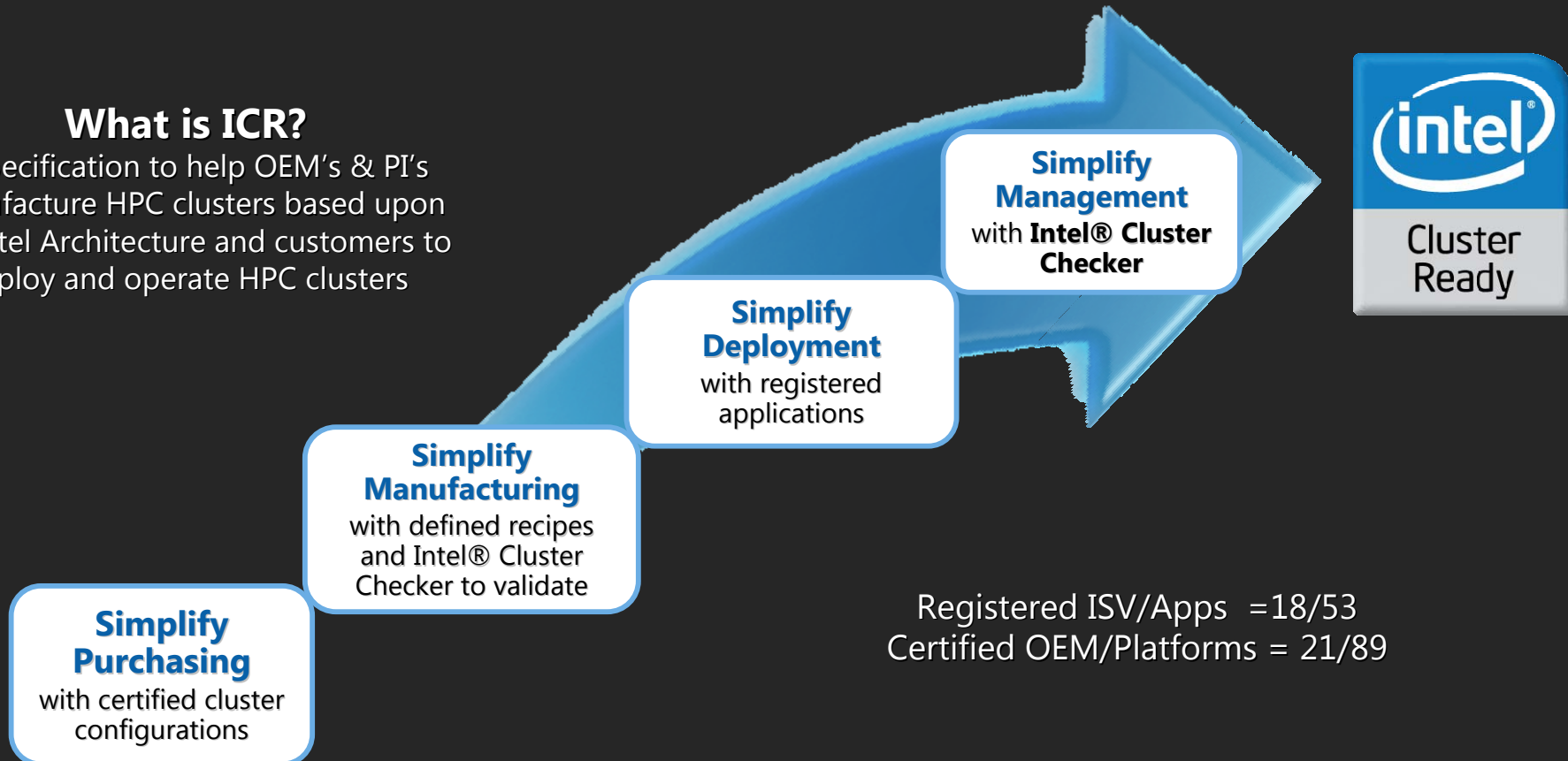
**Programmer Thinks Serially; Ct Exploits Parallelism**



# Intel® Cluster Ready Industry Program

## What is ICR?

A specification to help OEM's & PI's manufacture HPC clusters based upon the Intel Architecture and customers to deploy and operate HPC clusters



Registered ISV/Apps = 18/53  
Certified OEM/Platforms = 21/89

## Simplifying Your HPC-Cluster





# Solving Your HPC Challenges with Intel® Architecture

## Intelligent Performance

- Large performance gains to decrease time to discovery
- Improved power technology to provide a more energy efficient data center solution

## Software Versatility

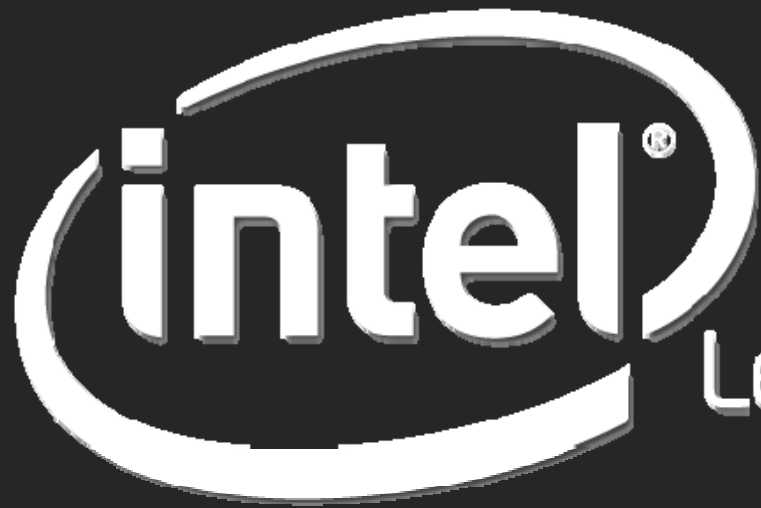
- Easily optimize application performance and eliminate the need to increase software resources
- Develop highly portable and scalable parallel software

## Deployment Ease of Use

- Certified cluster configurations to simplify cluster deployment

**Scaling Performance Forward**





Leap ahead™